

NASA TECH BRIEF



NASA Tech Briefs are issued to summarize specific innovations derived from the U.S. space program, to encourage their commercial application. Copies are available to the public at 15 cents each from the Clearinghouse for Federal Scientific and Technical Information, Springfield, Virginia 22151.

Simultaneous Message Framing and Error Detection

In binary code data transmission systems which are subjected to noise errors, suitable polynomial codes have been previously developed to provide a means for detecting and correcting these errors. In the prior systems utilizing polynomial codes, data bit sequences are encoded by dividing the data bits by a coding polynomial to obtain a quotient with a remainder. The remainder bits comprise the error checking bits and are transmitted following the data bits, the total comprising a message group consisting of n bits. This message is usually preceded by a series of framing bits which mark the beginning of the message. At the receiver, a framing signal obtained from the framing bits is required to clear the decoding circuits and to sense the beginning of a message. The decoder then proceeds to divide the message by the coding polynomial. The remainder of this division will be zero if no errors occurred during the message transmission. The separate framing signal is used in the prior systems to ensure that the decoder circuits are clear of errors caused by spurious noise in the data channel. Such framing wastes message space because a large number of bit positions must be allocated to enable reliable framing.

New message framing and error detection circuitry has been designed to provide a more practical and simplified system for the insertion of framing information in transmitted code groups. Separate message groups are framed without requiring framing bits in addition to error-checking bits. Another advantage is that the new circuitry separates any predetermined message sequence from other message sequences with-

out being hampered by intervening noise.

In one embodiment of the new circuitry, there is provided a shift register decoder for obtaining the remainder of the division of successively received, appropriately encoded message groups of n bits by a coding polynomial. An n -bit buffer stores the most recently received n bits. The contents of the shift register are continually updated by subtracting from the register the effect a bit received n -bit times earlier had on the contents of the shift register each time a new bit is received at the input of the shift register. Thus the shift register always contains the remainder obtained by dividing the contents of the n -bit buffer by the coding polynomial. Whenever the last preceding n bits received correspond to a message sequence, the remainder modulo coding polynomial is zero, or some preassigned pattern. The circuitry includes means for continuously testing the contents of the shift register for the preassigned test pattern of "ones" and "zeros." When the pattern appears, the contents of the buffer are gated to the output of the decoder.

Other advantages of the new circuitry are: (1) If synchronization with the incoming messages is lost because of an error condition, synchronization on the next received error-free message will automatically occur. (2) Separate test patterns may be assigned to different transmitters which may all transmit messages simultaneously. Messages associated with only one of several transmitters may be segregated by a decoder by merely selecting the test pattern used by that one transmitter.

(continued overleaf)

Note:

This circuitry should be of interest to designers and users of telemetry systems.

Patent status:

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to the International Business

Machines Corporation, 18100 Frederick Pike, Gaithersburg, Maryland 20760.

Source: A. H. Frey, Jr.
of IBM Corporation
under contract to
Manned Spacecraft Center
(MSC-12001)